Amendments to the Specification:

Replace the paragraph beginning at line 4 on page 14 with the following paragraph:

The host interface 122 may also function as a test interface controller (TIC) that provides a parallel test access port to the first and second processor 102 and 104, as well as the ASB 210. The TIC allows externally applied test vectors to be converted into internal bus transfers. More than one host interface 122 may be maintained by the cable modem device 100. For example, in addition to the host interface 122, a PCI or similar interface may added for communicating to a host system, while the host interface 122 communicates with other peripherals such as voice attachments. The host interface 122 supports a slave mode which provides an external host processor access to its internal memory, as well as memory-mapped register set. The host interface **[[112]]** **122** also supports a master mode which allows control signals to access external slave devices such as flash memory or data peripherals.

Replace the paragraph beginning at line 12 on page 19 with the following paragraph:

Messages from the message router 401 to the downstream process 404 are placed in a downstream process input message queue 424, while messages from the downstream process 404 to the message router 401 are placed in a downstream process output message queue 426. The downstream process 404 communicates with a downstream PHY **[[440]]** **444** via a downstream interface 446 and MPEG buffers 448. The downstream process 404 further utilizes a downstream DES/CRC engine 442 to provide decryption and validation functionality.